



# RS880PM-AM VER:1.0.

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AM3+ Stackup(1080 prepreg,4L)

Layer	Material	OZ	Hight(mm)	Hight(mil)	GECS	Intel-6
	Solder Mask		0.0254	1.00		
	Plating	1.0	0.0356	1.40	1.4~1.9	1.9
L1	Cu	0.5	0.0178	0.7		
	Dielectric (HRC)		0.0686	2.70		
L2	Cu	1.0/2.0	0.03555/0.0711	1.40/2.80		
	Dielectric		1.1379	44.8		
L3	Cu	1.0/2.0	0.03555/0.0711	1.40/2.80		
	Dielectric (HRC)		0.0686	2.70		
L4	Cu	0.5	0.0178	0.7		
	Plating	1.0	0.0356	1.40	1.4~1.9	1.9
	Solder Mask		0.0254	1.00		
	Total		1.5748			

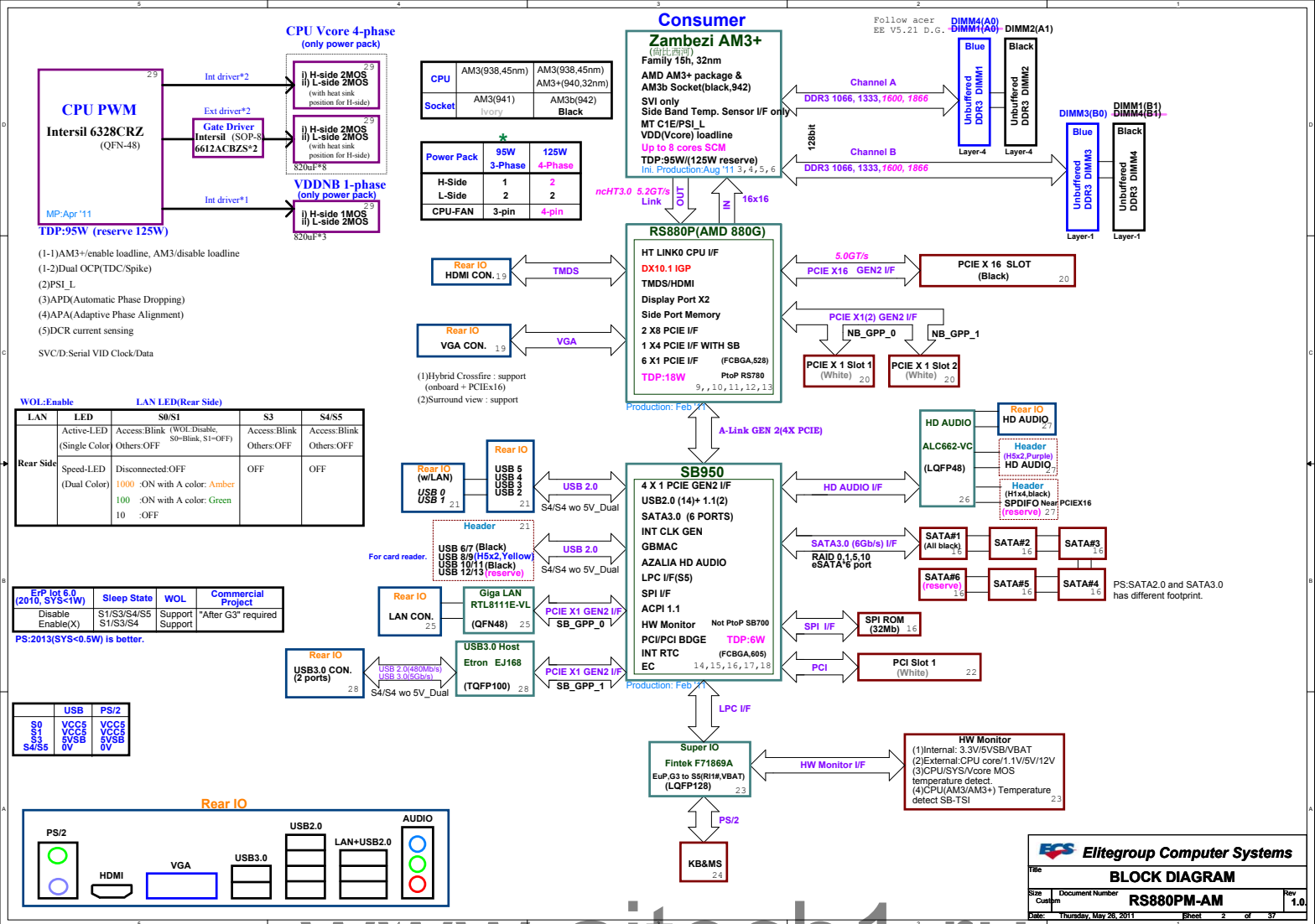
Job	Signature	Date
Schematics Designer	Dennis/Scott	03/08/'11~01/08/'11
Layout		03/08/'11
Approval		

PCB STACK: L1:TOP L2:PWR L3:GND L4:BOTTOM  
PCB Size : 244x244x1.6mm,4L(62mil=1.57mm),1080-prepreg

- (1)47079\_2\_02 AMD Family 15h Processor Electrical Data Sheet (NDA)\_2010-03-xx  
(2)46103\_rs880\_dg\_nda\_1.06 RS880-Series IGP Motherboard Design Guide (NDA)\_2010-09-07  
(3)48702\_sb9xx\_dg\_nda\_1.00 SB9xx Motherboard Design Guide (NDA)\_2010-08-20  
(4)Ref.Dory\_D (RS880P/SB950) Dory Schematic for AM3r2 (PDF)\_2010-11-29

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Cover Page			
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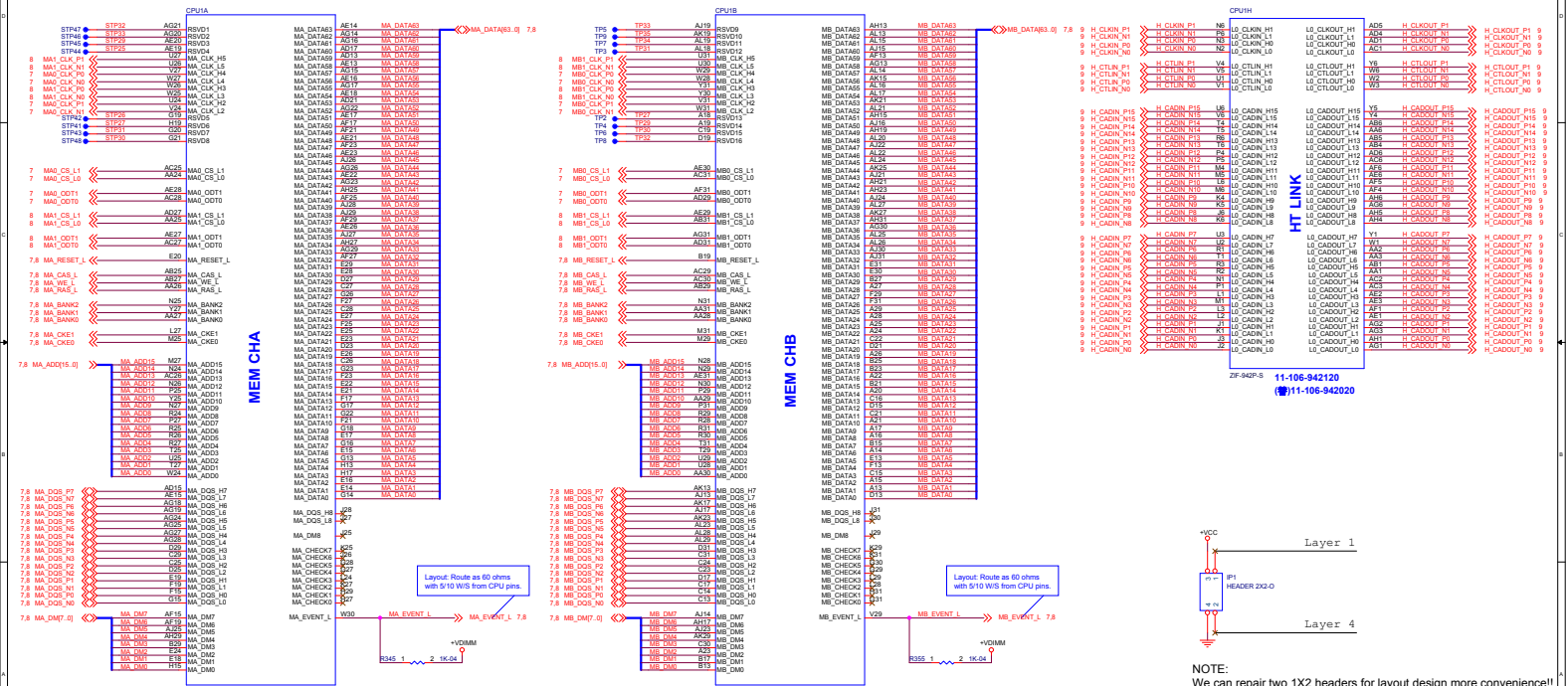
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## CPU Memory


## DDR3 Memory Interface A

## DDR3 Memory Interface B

HT LINK



NOTE:  
We can repair two 1X2 headers for layout design more convenience!!

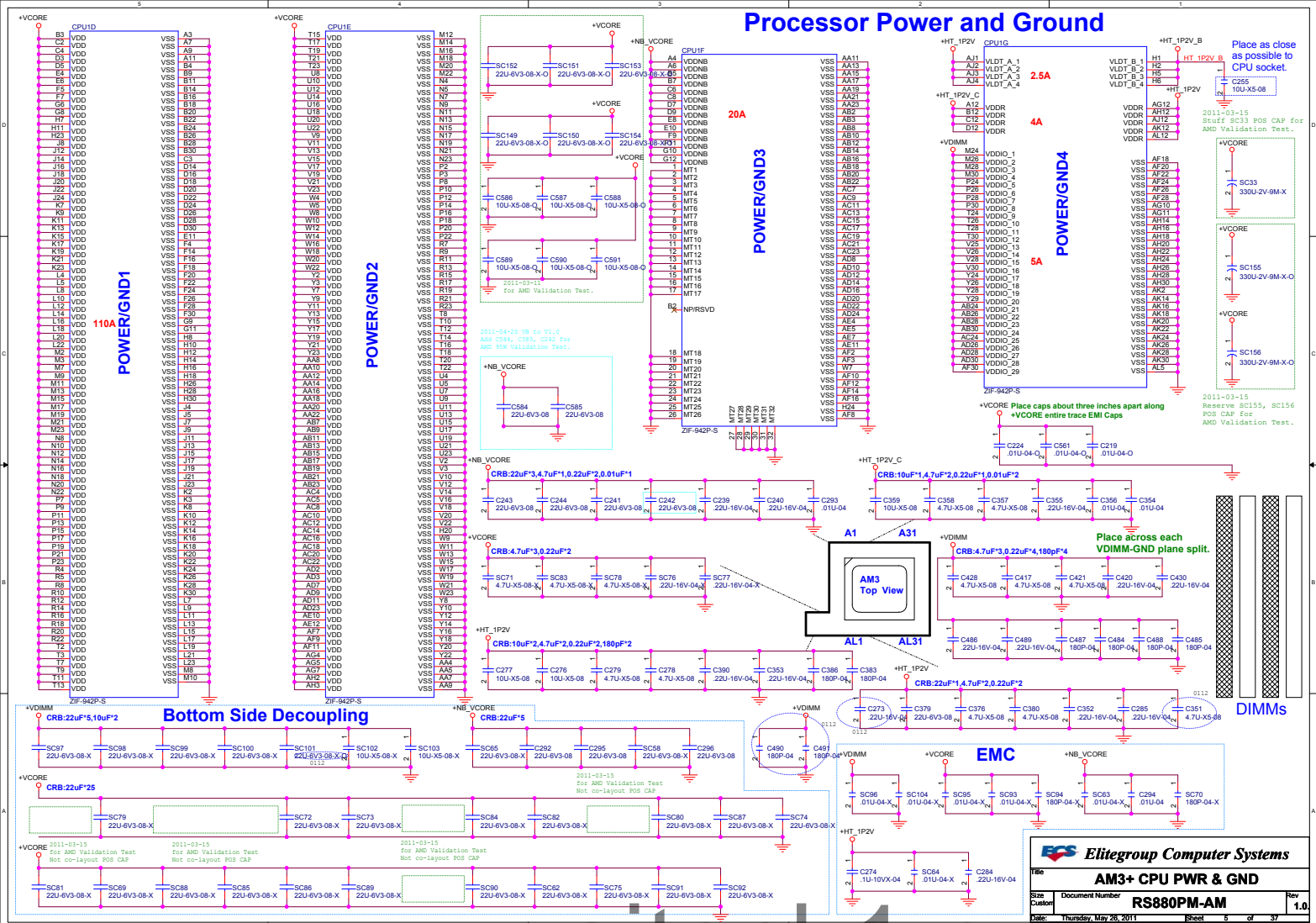
 <b>Elitegroup Computer Systems</b>		
<b>File</b> <b>HT,CPU MEMORY</b>		
<b>Size</b> 1024K	<b>Document Number</b> <b>RS880PM-AM</b>	<b>Rev</b> <b>1.0</b>
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## Processor Power and Ground

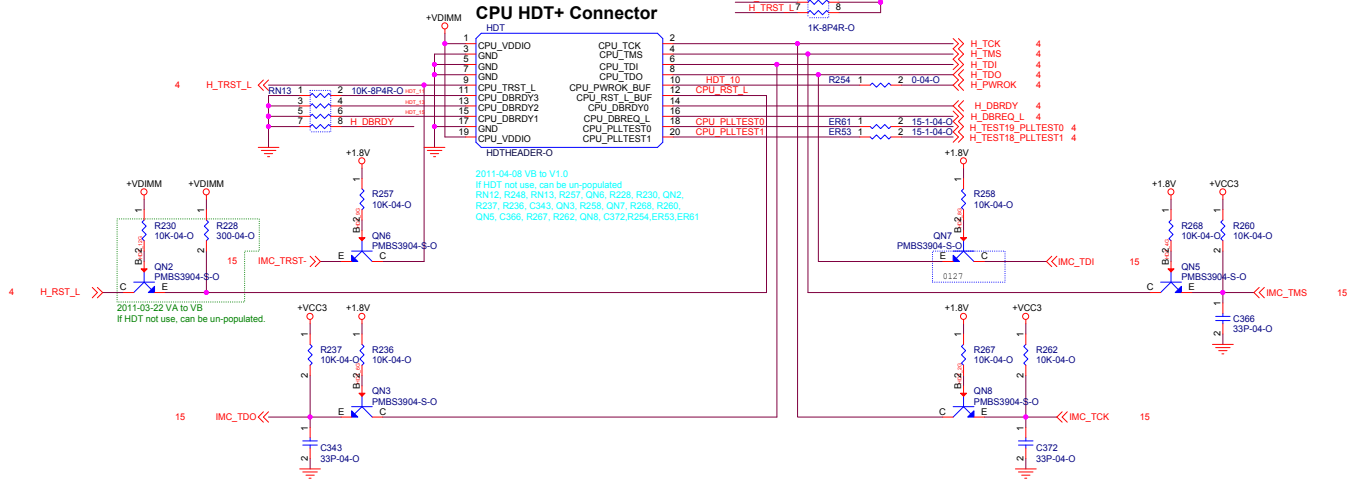


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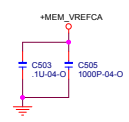
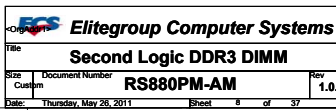
# HDT:Hardware Debug Tool

11-106-942120  
(☎)11-106-942020

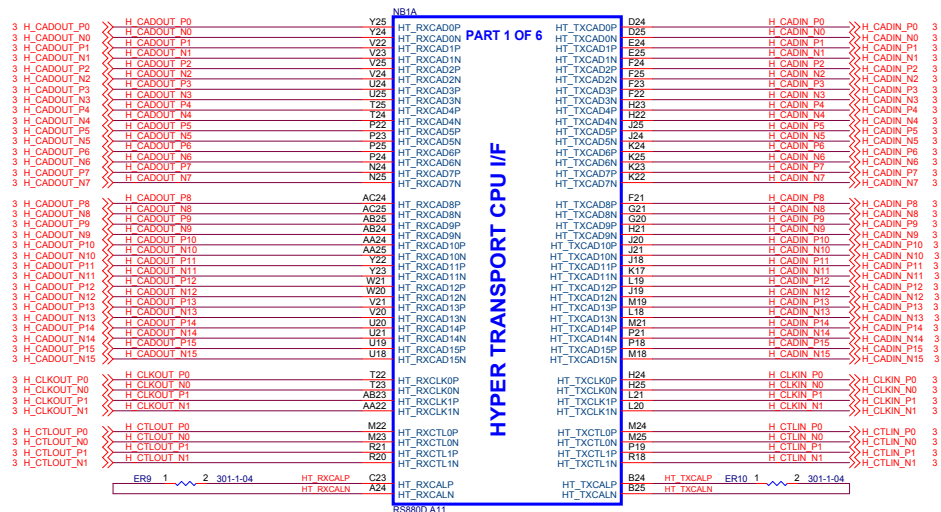
2011-03-08 VA to VB  
48121\_1\_02 AM3/2  
Processor Motherboard  
Schematic Checklist (NDA)  
2011-02-07.xlsx update.



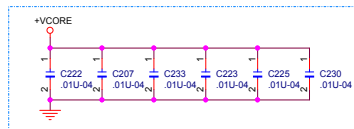








HT LINK STITCHING CAPS.



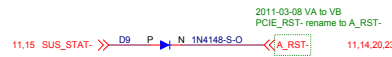
<b>RS880P-HT LINK I/F</b>			
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## RS880P STRAPS



### RS880P: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
 ★ 1: Bypass the loading of EEPROM straps and use Hardware Default Values  
 0: I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
 RS880P: pin SUS\_STAT#



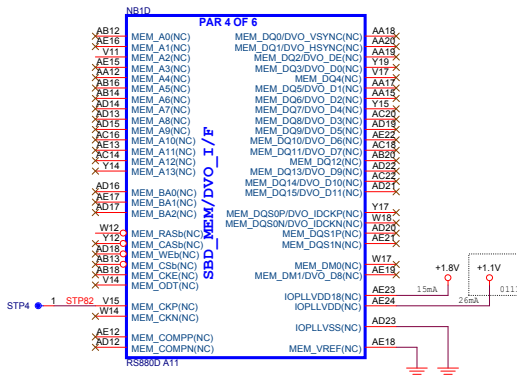
### RS880P: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO  
 ★ 1: Disable (RS740/RS780); Enable (RX780)  
 0: Enable (RS740/RS780); Disable (RX780)  
 RS880P: pin VSYNC



### RS880P: SIDE-PORT MEMORY ENABLE

Enables Side port memory  
 ★ 1: Disable (RS880P)  
 0: Enable (RS880P)  
 RS880P: pin HSYNC



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RS880P-SPMEM/STRAPS			
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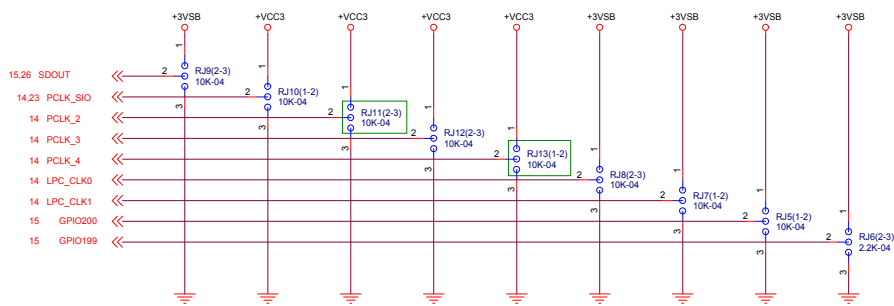












This strap is not used if the strap CLKGEN is configured for external clock generator mode.

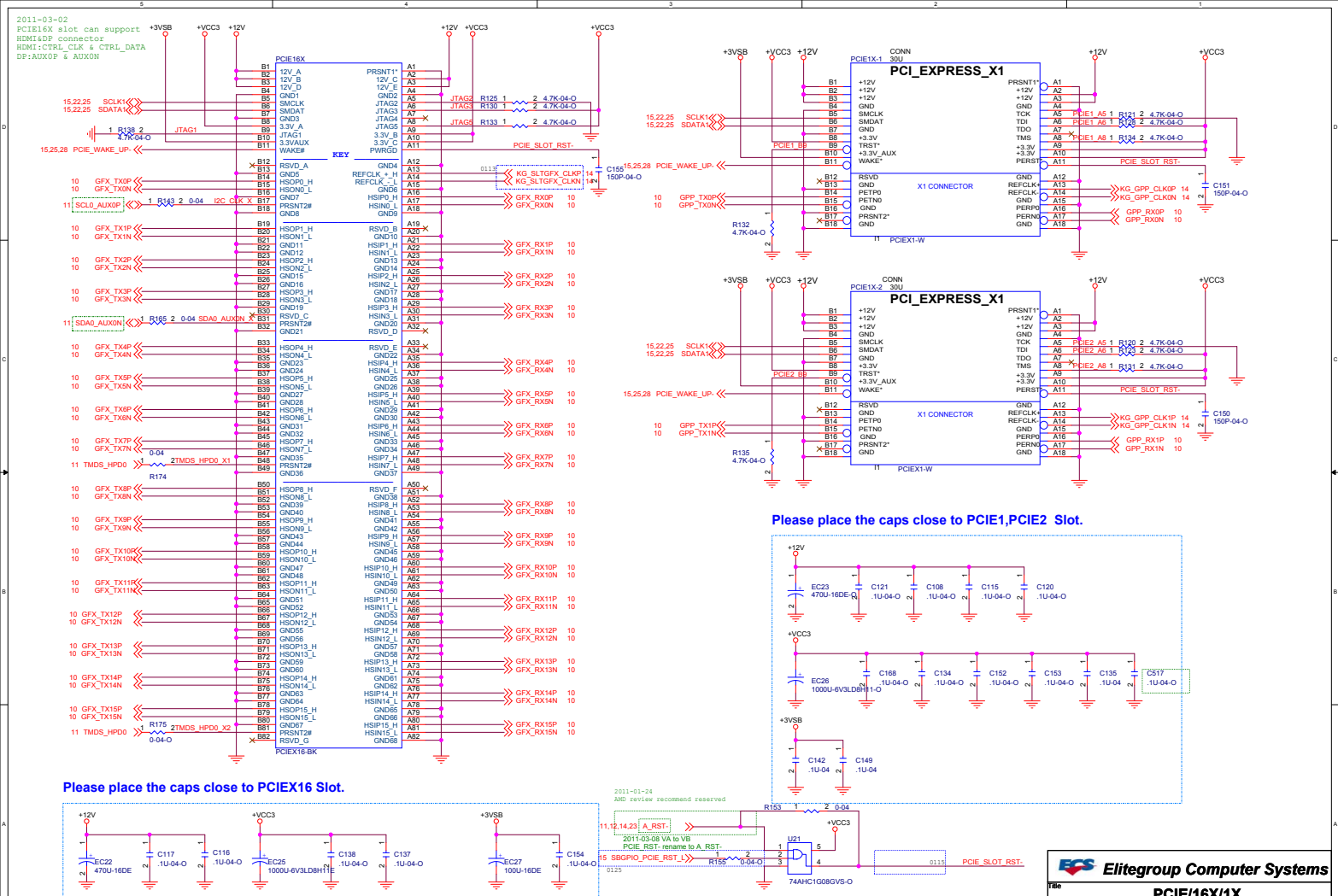
## REQUIRED STRAPS

	AZ_SDOUT	PCLK_SIO	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GP200	GP199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2 ★ DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	Required setting for integrated clock mode ★ DEFAULT	EC ENABLED	Internal CLOCK MODE ★ DEFAULT	ROM TYPE: H, H = Reserved H, L = SPI ROM ★ DEFAULT	
PULL LOW	Performance Mode ★ DEFAULT	FORCE PCIE GEN1	Watchdog Timer Disabled ★ DEFAULT	IGNORE DEBUG STRAP ★ DEFAULT	Reserved	EC DISABLED ★ DEFAULT	External CLOCK MODE	L, H = LPC ROM L, L = FWH ROM	

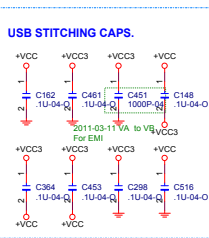
File		
SB950 STRAPS		
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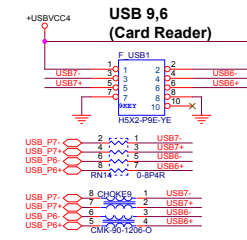




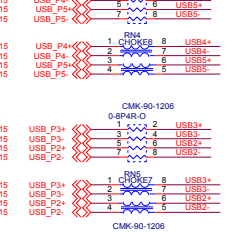
### USB STITCHING CAPS.



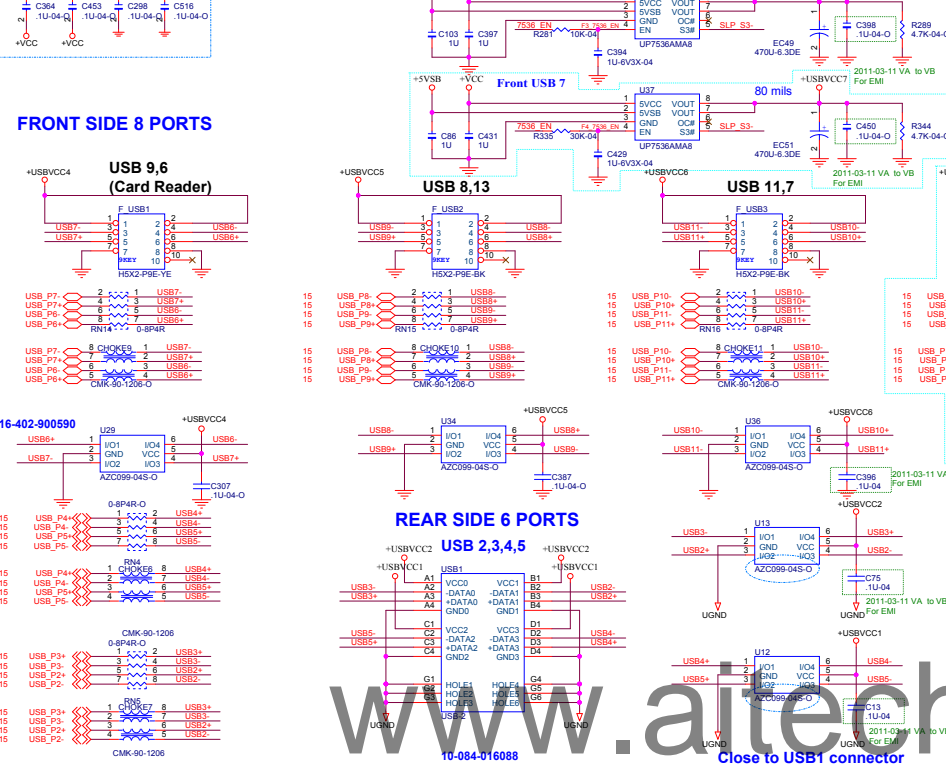
**USB 9,6**



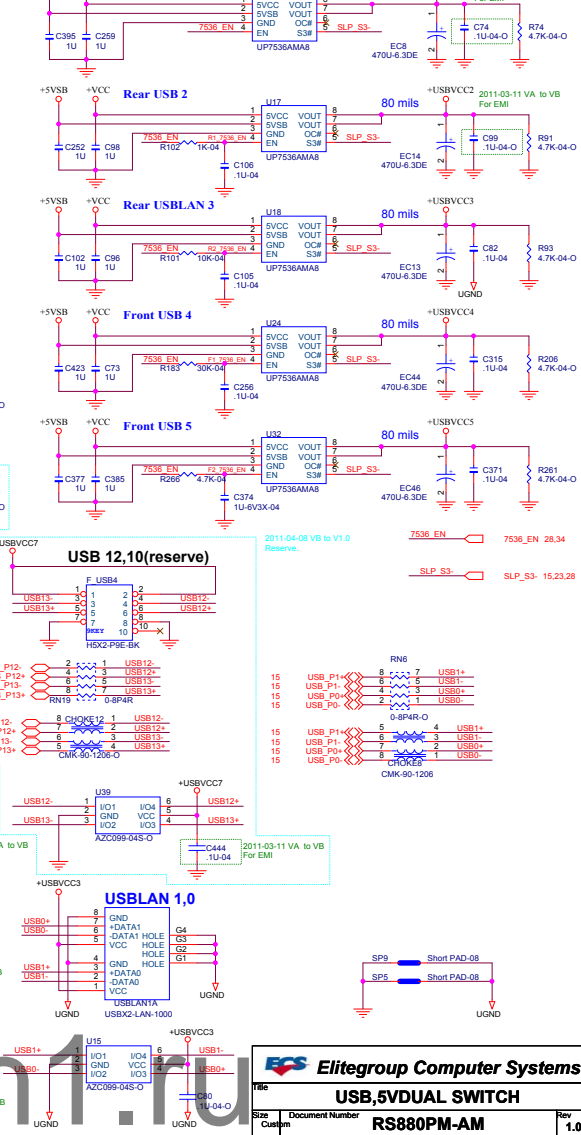
**USB 2,3,4,5**

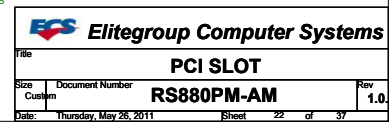


## 80




73 7536 EN  
R183 30

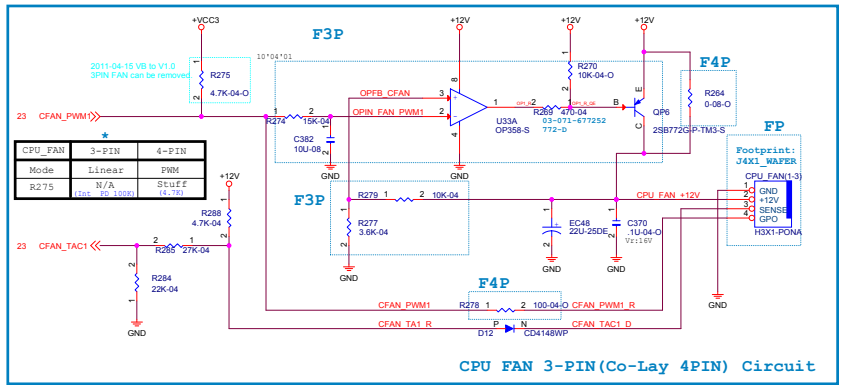
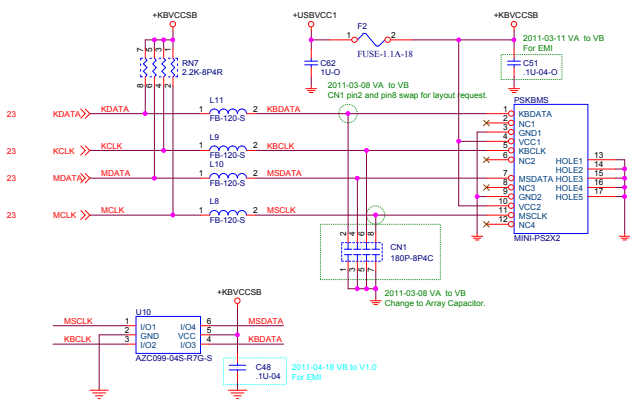




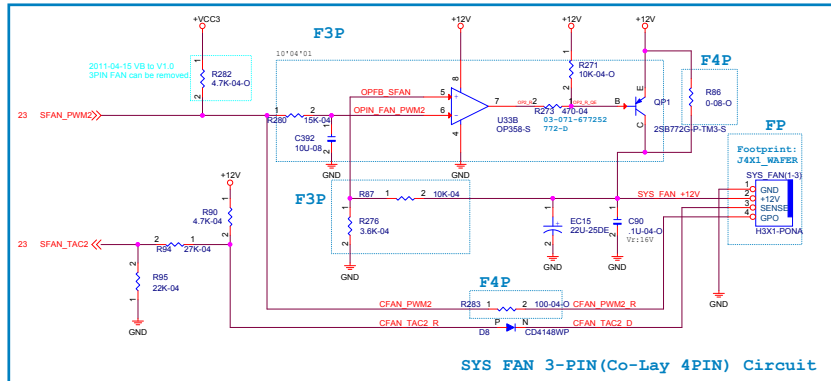
2011-04-01 VB to V1.0  
+RTCVCC rename to +VBAT\_IO

 <b>Elitegroup Computer Systems</b>			
Title			
<b>SIO - F71869A</b>			
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## PS2



CPU FAN: 3PIN (95W) , 4PIN (125W)				
MODE	F3P	F4P	FP Value	R275
3PIN	V	X	H3X1-PONA	X
4PIN	X	V	H4X1-PONA	V



SYS FAN				
MODE	F3P	F4P	FP Value	R282
3PIN	V	X	H3X1-PONA	X
4PIN	X	V	H4X1-PONA	V

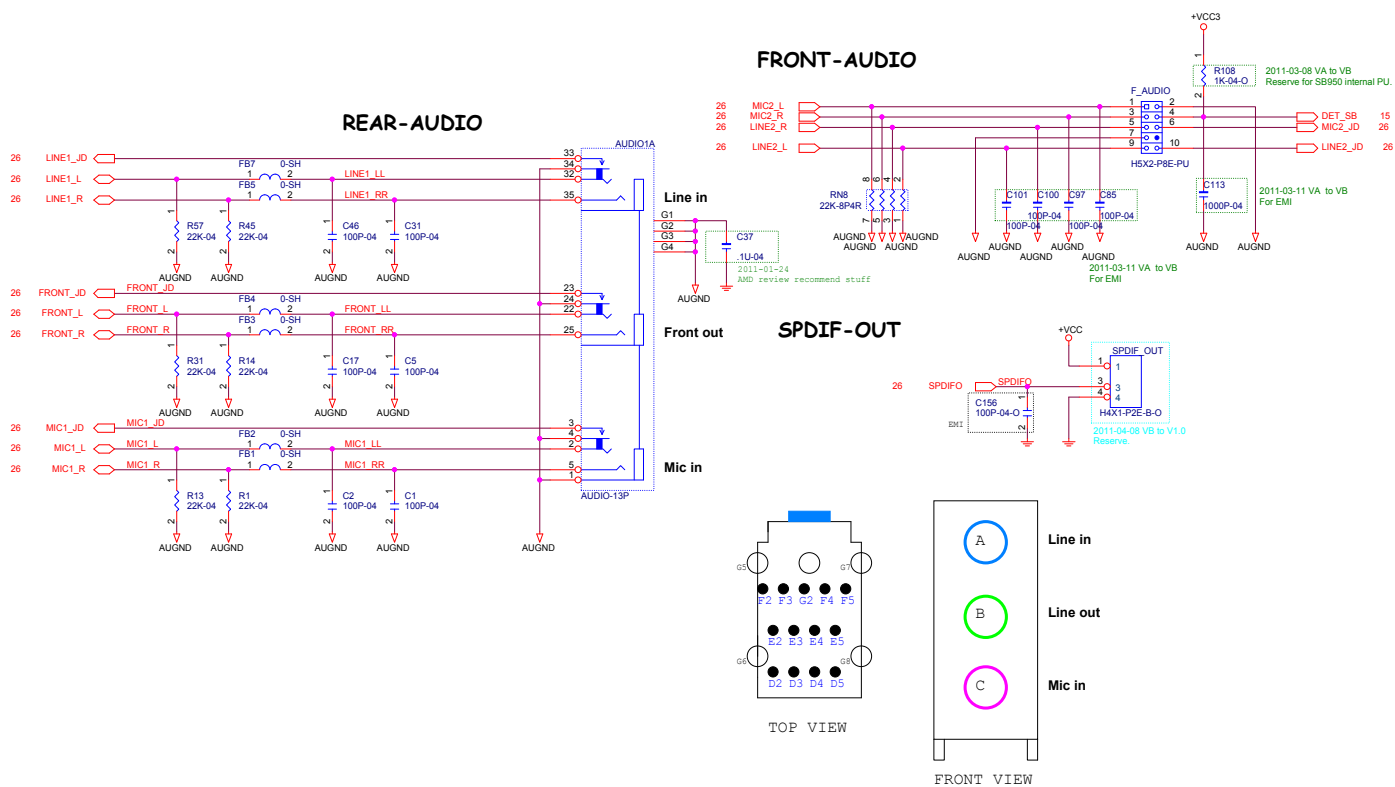
Elitegroup Computer Systems	
FAN,PS2,FAN	
File	Customer
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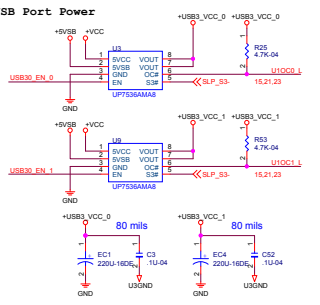
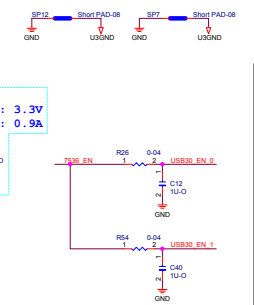
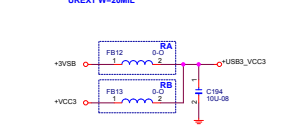
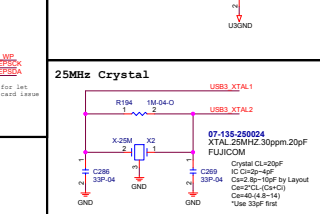
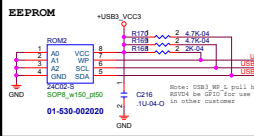
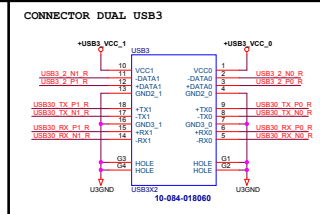







<b>AUDIO ALC662 (PANEL)</b>			
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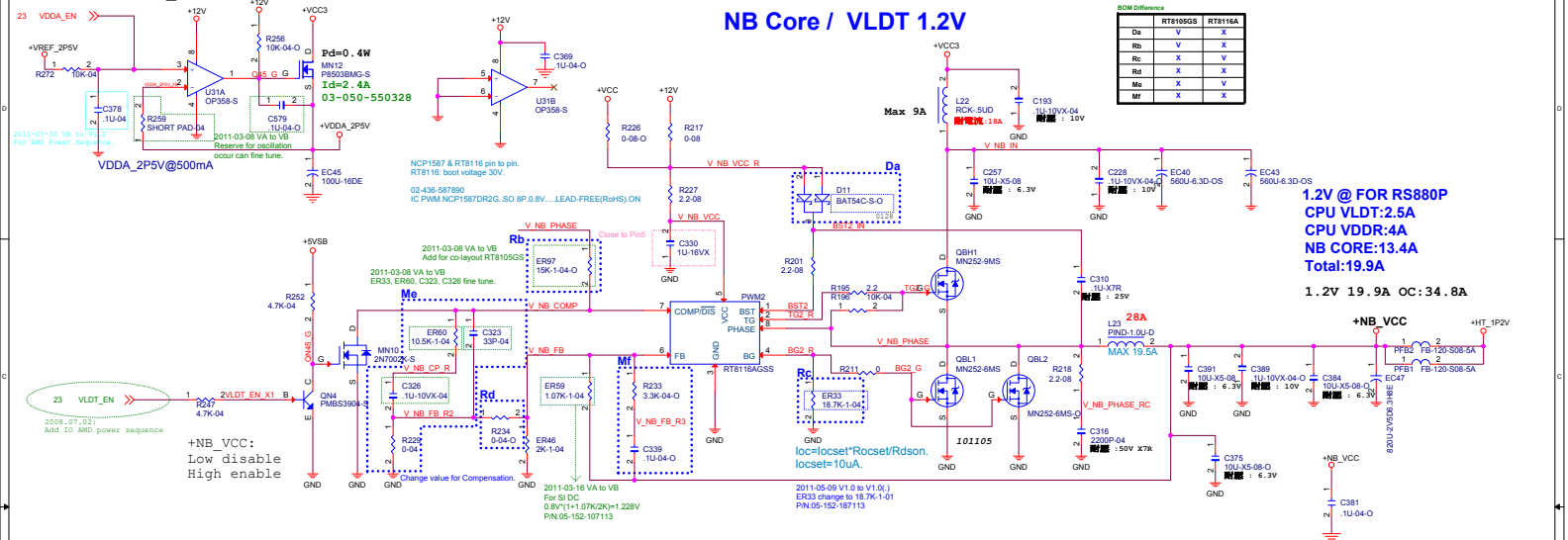
 <b>Elitegroup Computer Systems</b>			
<b>EJ168 USB3.0 HOST</b>			
Size Custom	Document Number <b>RS880PM-AM</b>		Rev 1
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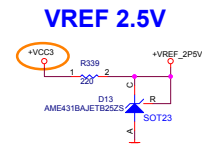
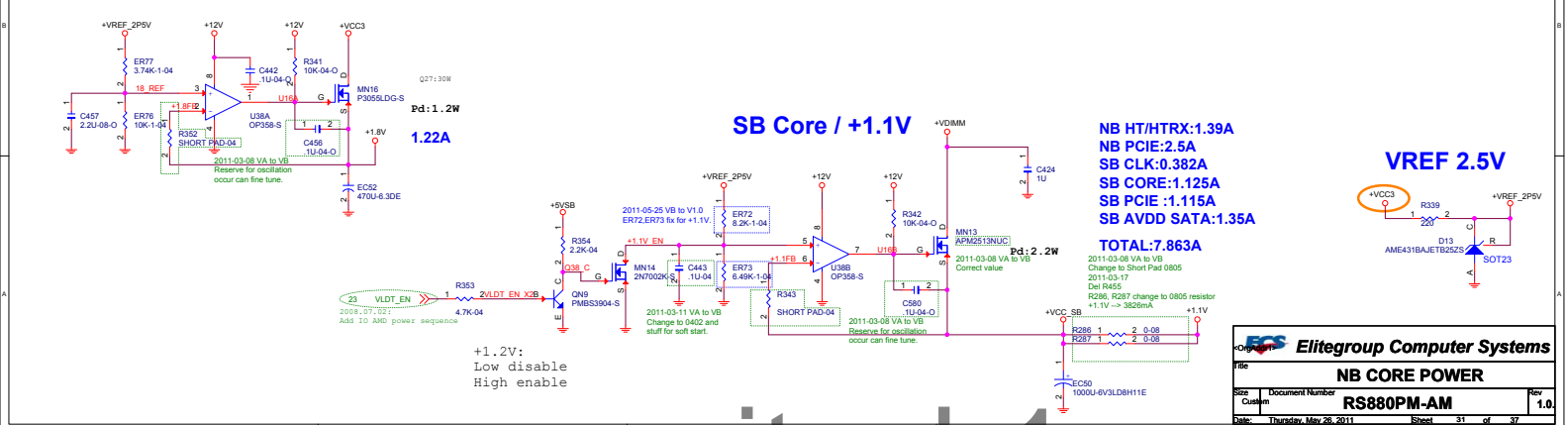


**NB Core / VLDT 1.2V**

	RTS105GS	RTS115
Da	V	X
Rb	V	X
Rc	X	V
Rd	X	X
Me	X	V
Mf	X	X

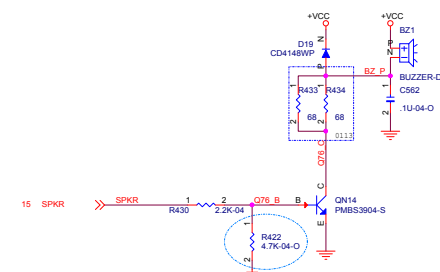
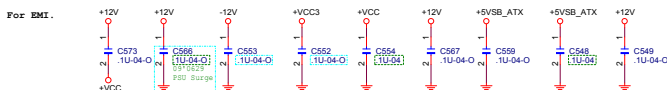


**+1.8V**



NB HT/HTRX:1.39A  
 NB PCIE:2.5A  
 SB CLK:0.382A  
 SB CORE:1.125A  
 SB PCIE :1.115A  
 SB AVDD SATA:1.35A  
 TOTAL:7.863A

 <b>Elitegroup Computer Systems</b>			
File			
<b>NB CORE POWER</b>			
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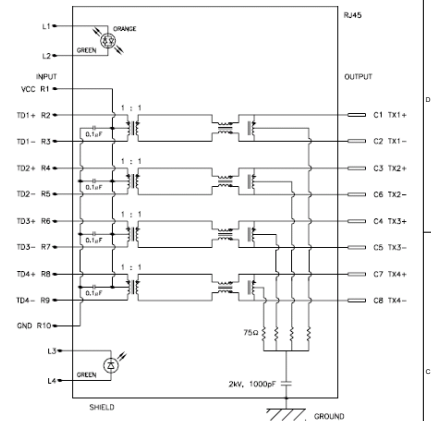
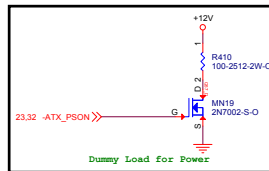
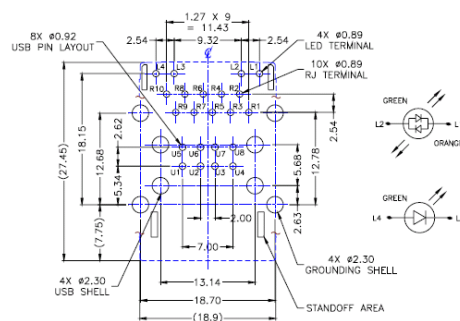


F71869A				
Name	Type	Voltage	Functional Description	Net
RI1#	I	3VSB	WOL	_RIA
GPIO31	I/O	VCC3	reserve	GPIO31
GPIO32	I/O	VCC3	reserve	GPIO32
GPIO33	I/O	VCC3	reserve	GPIO33
GPIO34	I/O	VCC3	reserve	GPIO34
GPIO35	I/O	VCC3	reserve	GPIO35
GPIO02	I/O	3VSB	for Acer reserve	GPIO_02
GPIO03	I/O	3VSB	for Acer reserve	GPIO_03
GPIO15(LEDVSB)	I/O	3VSB	LED2	G_LED2
GPIO16(LEDVCC)	I/O	3VSB	LED1	G_LED1
OVT#	O	3VSB	to SB TALERT#	THRM_L
GPIO21	I/O	3VSB(5V )	reserve for UP7536 control	GPIO21
CTRL0#	OD	3VSB(5V )	for Eup control	CTRL0_L
S3_GATE1	OD	3VSB(5V )	for S3 VDIMM DUAL power control	ST1

Name	Type	Voltage	Functional Description	Net
RT1#	I	3VSB	WOL	-R1A
GPIO31	I/O	VCC3	reserve	GPIO31
GPIO32	I/O	VCC3	reserve	GPIO32
GPIO33	I/O	VCC3	reserve	GPIO33
GPIO34	I/O	VCC3	reserve	GPIO34
GPIO35	I/O	VCC3	reserve	GPIO35
GPIO02	I/O	3VSB	for Acer reserve	GPIO_02
GPIO03	I/O	3VSB	for Acer reserve	GPIO_03
PIOT15/LEDVSB	I/O	3VSB	LED2	G_LED2
GPIO16/LEDVCC	I/O	3VSB	LED1	G_LED1
OVT#	O	3VSB	to SB TALERT#	THRM_L
GPIO21	I/O	3VSB(5V)	reserve for UP7536 control	GPIO21
CTRL0#	OD	3VSB(5V)	for Eup control	CTRL0_L
S3_GATE1	OD	3VSB(5V)	for S3 VDIMM DUAL power control	ST1

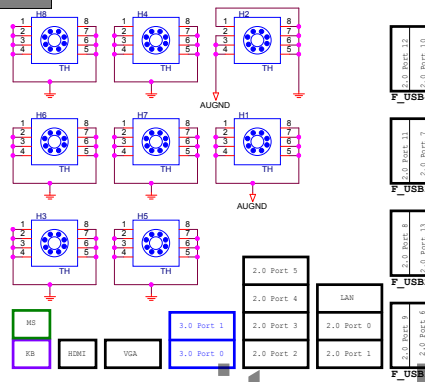
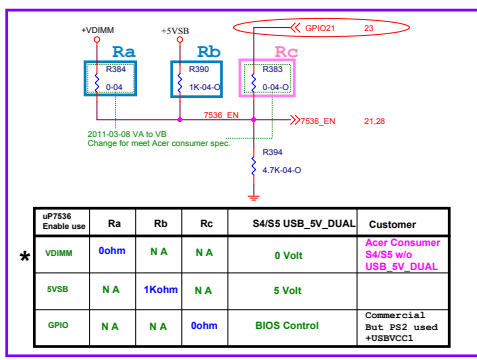
### NB\_PWRGOOD Sequence

PS/2 Keyboard		Consumer	
BIOS Option	System State	Eup Lot "Disabled"	Eup Lot "Enabled"
Disable	S1/S3	N	N
	S4/S5	N/A	N/A
	After G3	N/A	N/A
Enable	S1/S3	Y	Y
	S4/S5	N/A	N/A
	After G3	N/A	N/A
S1/S3 Wakeup (If support)	S1/S3	N/A	N/A
	S4/S5	N/A	N/A
	After G3	N/A	N/A
S4/S5 Wakeup (If support)	S1/S3	N/A	N/A
	S4/S5	N/A	N/A
	After G3	N/A	N/A
USB Keyboard & Mouse		Consumer	
BIOS Option	System State	Eup Lot "Disabled"	Eup Lot "Enabled"
Disable	S1/S3	N	N
	S4/S5	N/A	N/A
	After G3	N/A	N/A
Enable	S1/S3	Y	Y
	S4/S5	N/A	N/A
	After G3	N/A	N/A
S1/S3 Wakeup (If support)	S1/S3	N/A	N/A
	S4/S5	N/A	N/A
	After G3	N/A	N/A
S4/S5 Wakeup (If support)	S1/S3	N/A	N/A
	S4/S5	N/A	N/A
	After G3	N/A	N/A

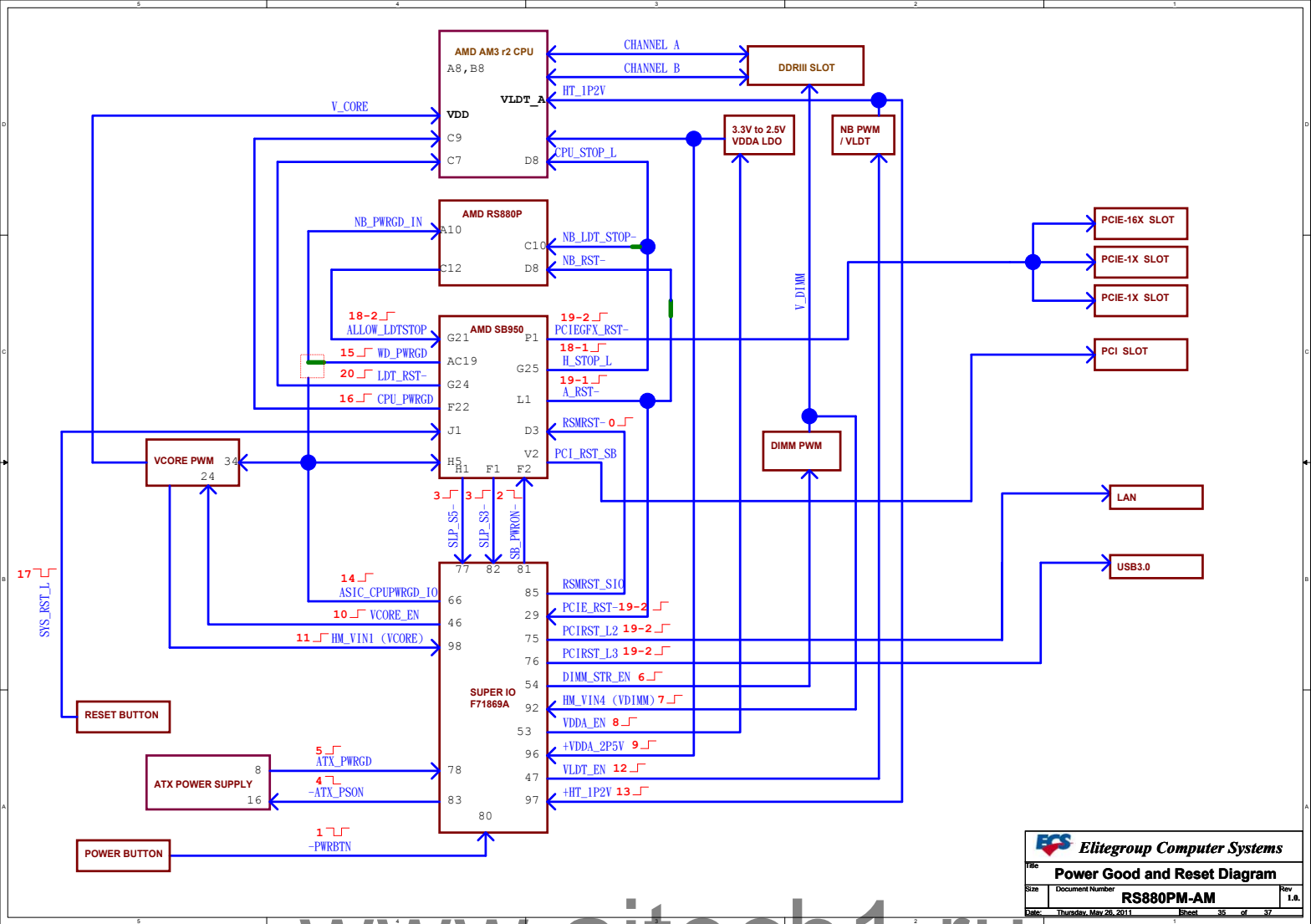


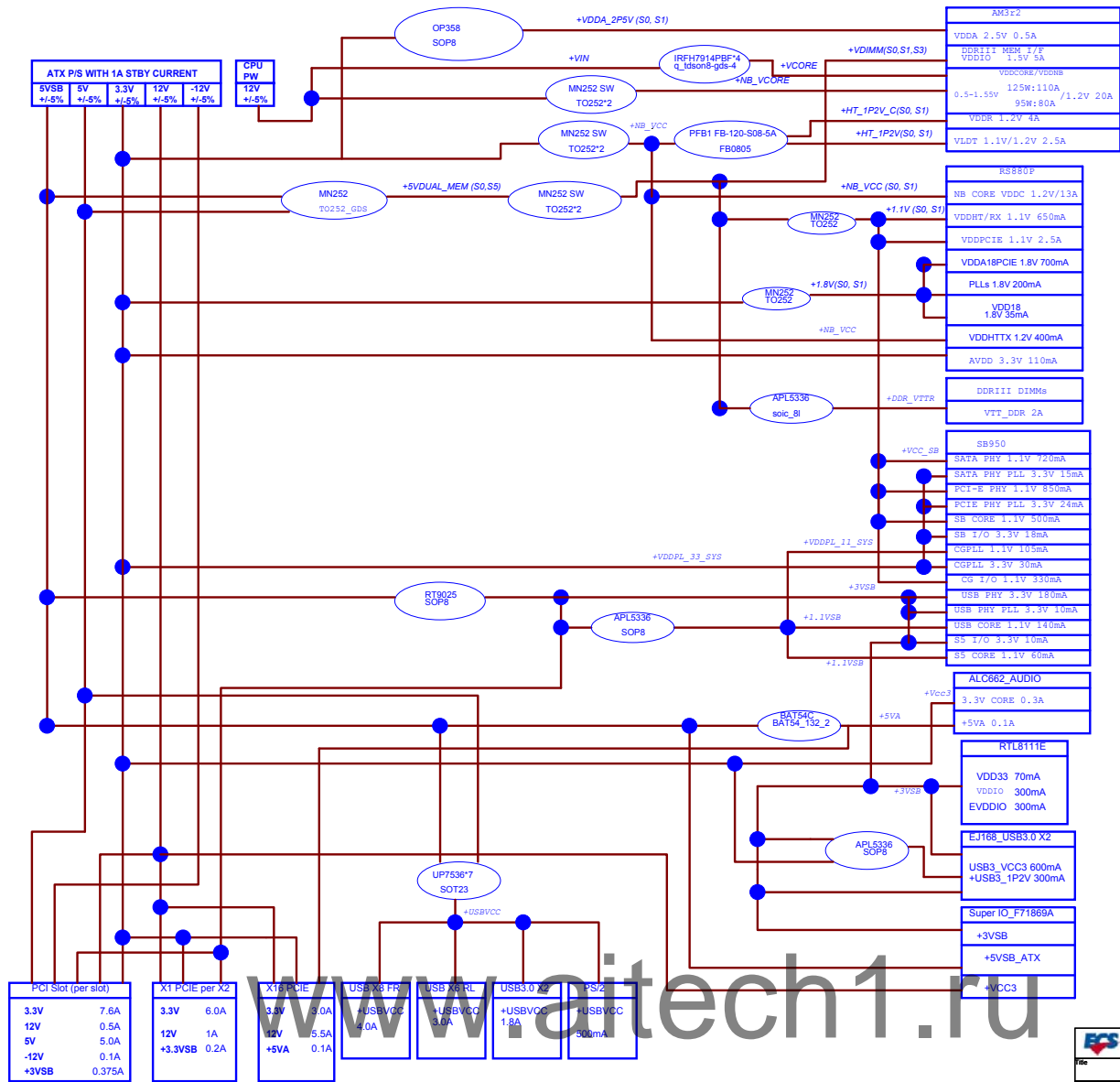
2011-03-15 VA to VB  
Reserve for reset issue

## POWER GOOD &amp; ENABLES




 <b>Elitegroup Computer Systems</b>	
Title	
<b>Power Sequence</b>	
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REVISION HISTORY:

	Date	Notes	Rev	Date	Notes	
A	2011-01		1.0	2011-04-21	Page 04 Del MN6,MN8,MN9, add U26,U27,U30 for PWROK, LDT_RST#, LDT_STOP# Rising Time.	
B	2011-03-08	Page 04 Net name SCLK3, SDATA3 change to SIC, SID. R202, R208, R212 change to Short Pad. R186 stuff for AM3 compatible. Add DRPCTRL circuit. Page 05 For AMD Validation fine tune. Del SC59,SC60,SC61,SC66,SC67,SC68 Add C584-C591, SC149-SC154 SC33,SC155,SC156 (POS CAP 330uF) Page 06 R248 change to 1K-04 for AM3r2 Schematic Checklist update. R228 R230 QN2 can be un-populated. Page 10 +NB_VCC change to +VDD_PCIE Page 11 R136, SR1 change to Short Pad. Reserve SC148 for meet Dory CRB. PCIE_RST- rename to A_RST- +NB_VCC change to +VDD_PCIE Del R106,R113 Add R107,U20 for Sequence. Page 12 PCIE_RST- rename to A_RST- RJ2,RJ3 change to 5% resistor. Page 13 Add +VDD_PCIE Page 14 PCIE_RST_GFX- rename to PCIE_RST- PCIE_RST- rename to A_RST- A_RST- rename to A_RST R337,R340 change to 22-04 C434,C437 stuff for SI Page 15 R345 not stuff because SB950 have internal PU. Stuff C416 for SI. Page 16 SATA1-SATA6 change PCB footprint to 2.0 type. Page 19 C11 not stuff. C45 stuff for EMI C24,C25 change to 47pF for I2C rising time Page 20 PCIE_RST- rename to A_RST- C13,C74,C75,C99,C396,C398,C444,C450,C451 for EMI Page 21 C13,C74,C75,C99,C396,C398,C444,C450,C451 for EMI Page 22 C393,C399 for EMI Page 23 PCIE_RST- rename to A_RST- Net name SCLK3, SDATA3 change to SIC, SID. Net name TSI_CLK, TSI_SDA change to TSI_SCLK, TSI_SDATA. Page 24 C68, C69, C70, C71 change to CN1. CN1 Pin2 and Pin8 swap for layout modify. C51 for EMI Page 25 PCIE_RST_GFX- rename to PCIE_RST- R71 for onboard LAN S3/S4/S5 WOL C58 for EMI	Page 26 R84, R92 change to Short Pad. Page 27 Reserve R108 for SB950 internal PU. C85,C97,C100,C101,C113 for EMI Page 28 PCIE_RST_GFX- rename to PCIE_RST- Del RN1, RN2 Page 29 SR31 reserve for VGA noise. C581,C582 reserve for +VCC noise interference PS/2 signal. C583 reserve stitching capacitor. L26 co-layout L16 for 95W solution. Design change for AMD Validation Test, please refer to p.29 . Page 30 Design change for Validation Test, please refer to p.30. EC55,EC59 change value and footprint. ER68 change to 3.9K for DC. Page 31 Reserve R259,R343,R352,C456,C579,C580 for oscillationoccur can fine tune. ER9 change to 1.07K for DC. C443 stuff for soft start. Page 32 R373 chane to 130-04 for LED current fix. Page 33 NB Heat Sink chane Height to 25mm P/N:20-120-011492 Page 34 Del R363, add R384 for meet Acer consumer spec. Reserve D22 for reset issue.	1.0	2011-05-12	Page 04 Change U26,U27,U30 to 74AUP1G07GW for PWROK, LDT_RST#, LDT_STOP# Rising Time. Add MN21,MN22,R461,ER102 for PWM Offset control. Page 11 Change U19 to 74AUP1G07GW and add R111 for AMD Power Sequence. Page 14 Add C433,C435,SR22,SR23 (USB3.0 change to stuff). C413,C414 change to 27P-04 for dynamic RTC. Del D23 and add R461 for follow AMD DG. Page 23 Add D27 to prevent voltage flow backward. Page 28 USB3.0 change to stuff. Page 29 Del ER50 for Offset control. Page 31 ER33 change to 18.7K-1-04 for OCP. ER72 change to 8.2K-1-04 ER73 change to 6.49K-1-04 for +1.1V.

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